FIG. 1

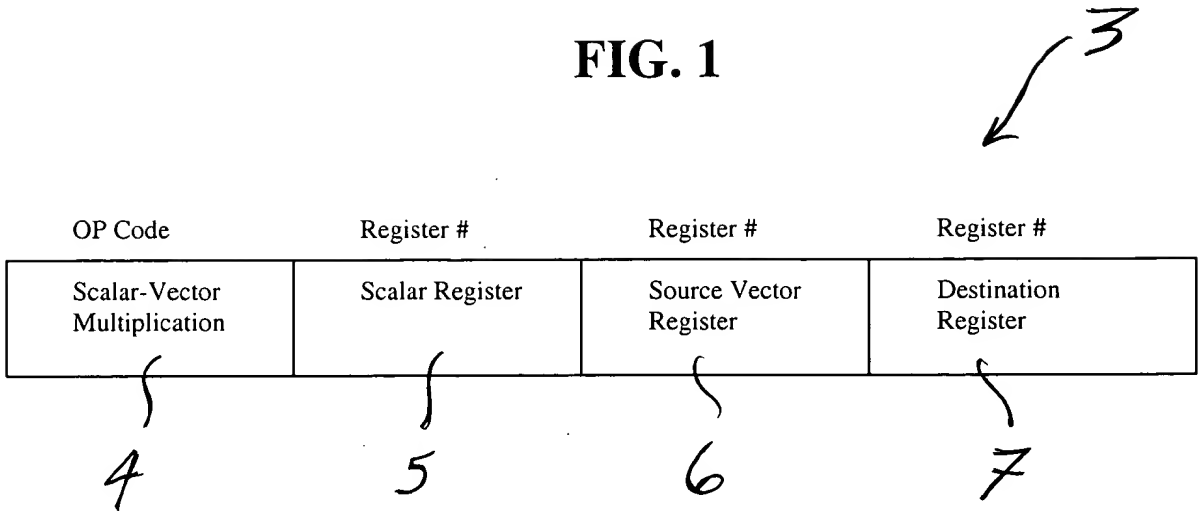
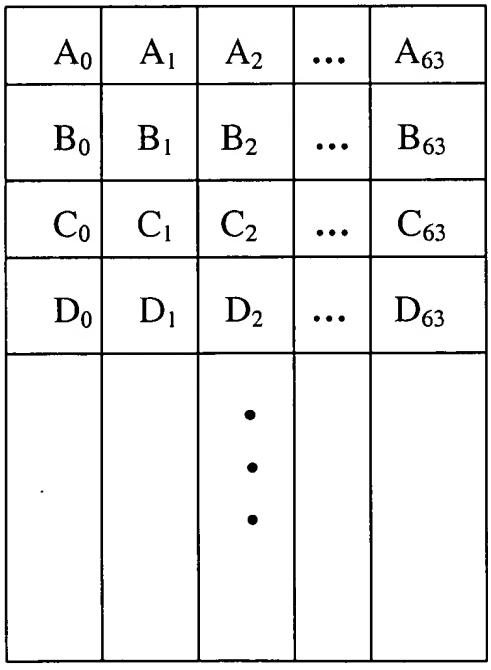

3
OP Code
Register #
Register #
Register #
Scalar-Vector Multiplication
Scalar Register
Source Vector Register
Destination Register
4
5
6
7

FIG. 2


2
A_0 A_1 A_2 ... A_{63}
B_0 B_1 B_2 ... B_{63}
C_0 C_1 C_2 ... C_{63}
D_0 D_1 D_2 ... D_{63}

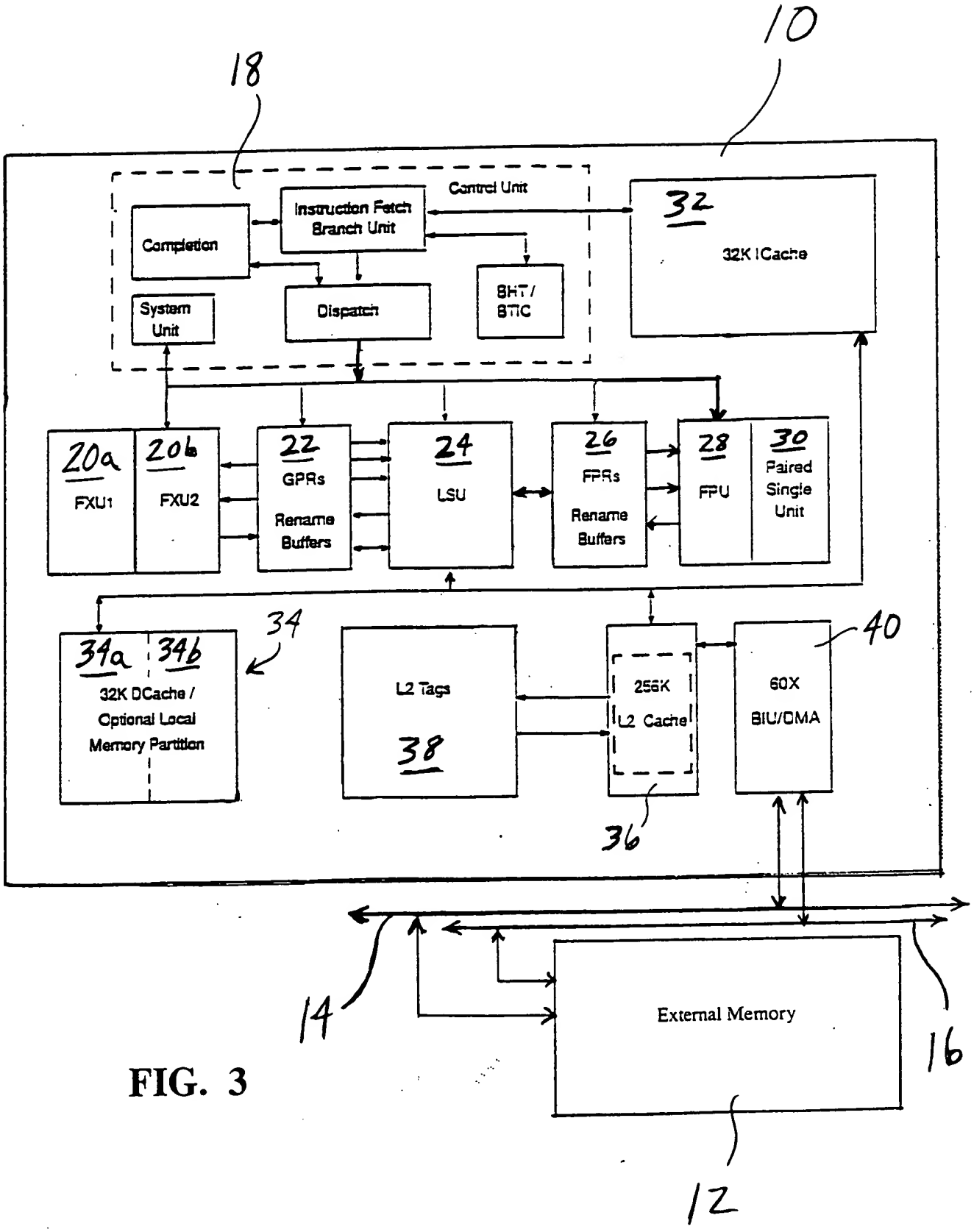

10
18
Control Unit
Instruction Fetch Branch Unit
Completion
System Unit
Dispatch
BHT / BTIC
32
32K ICache
20a
FXU1
20b
FXU2
22
GPRs
Rename Buffers
24
LSU
26
FPRs
Rename Buffers
28
FPU
30
Paired Single Unit
34
34a
34b
32K DCache / Optional Local Memory Partition
L2 Tags
38
256K L2 Cache
36
40
60X BIU/DMA
14
External Memory
16
12

FIG. 3

HID2 register bit settings

Bit(s)	Name	Description
0	LSQE	Load/Store quantized enable (non-indexed format) 0 psq_l[u] and psq_st[u] instructions are illegal 1 psq_l[u] and psq_st[u] instructions can be used
1	WBE	Write buffer enable 0 write buffer is disabled 1 write buffer enabled to gather non-cacheable data
2	PSE	Paired singles enabled 0 paired singles instructions are illegal 1 paired singles instructions can be used
3	LCE	Locked cache enable 0 Cache is not partitioned - 32 kB of normal cache 1 Cache is partitioned - 16 kB of normal cache and 16 kB of locked cache available
4-7	DMAQL	DMA queue length (read only) the number of used queue positions in the DMA, from 0 (queue empty) to 15 (queue full)
8-31	-	Reserved

FIG. 4

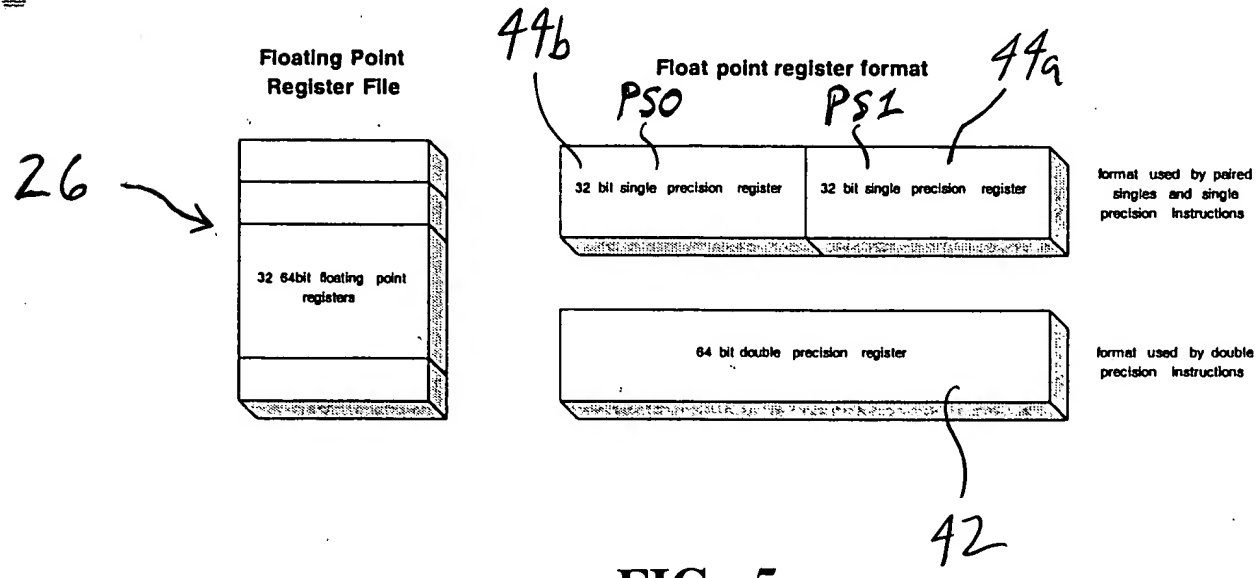


FIG. 5

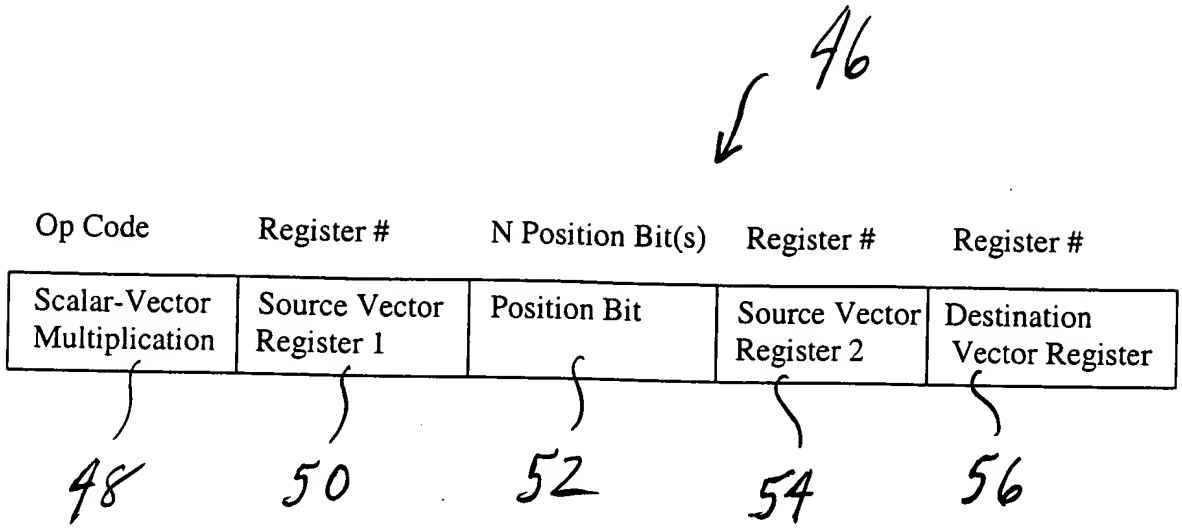


FIG. 6

ps_addx

Paired Single Add

ps_add **frD, frA, frB** (Rc = 0)

ps_add. **frD, frA, frB** (Rc = 1)

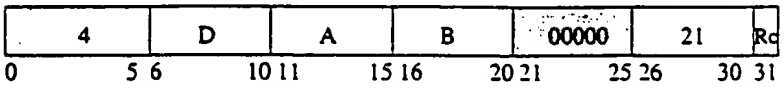


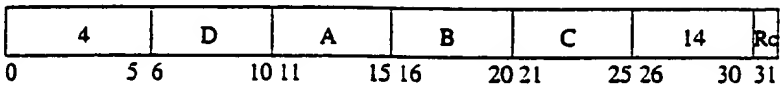
FIG. 7

ps_madds0*x*

Paired Single Multiply-Add Scalar High

ps_madds0 frD,frA,frC,frB (Rc = 0)

ps_madds0. frD,frA,frC,frB (Rc = 1)



frD_ps0 = frA_ps0 * frC_ps0 + frB_ps0

frD_ps1 = frA_ps1 * frC_ps0 + frB_ps1

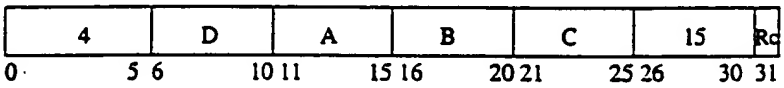
FIG. 8

ps_madds1*x*

Paired Single Multiply-Add Scalar Low

ps_madds1 frD,frA,frC,frB (Rc = 0)

ps_madds1. frD,frA,frC,frB (Rc = 1)



frD_ps0 = frA_ps0 * frC_ps1 + frB_ps0

frD_ps1 = frA_ps1 * frC_ps1 + frB_ps1

FIG. 9